

REMARKS

Claims 1-31 are presently pending. Claims 1, 3-7, 15, 19, 21, 23-25 and 27 have been amended. Claims 30 and 31 have been added. Claims 11-13, 15-17, 22, 23, 25 and 27-29 have been withdrawn as being drawn to non-elected species. Applicants reserve the right to file one or more divisional applications in order to prosecute claims directed to the non-elected species, if necessary.

Applicants respectfully request reconsideration of the application in view of the foregoing amendments and the remarks appearing below.

Rejection under 35 U.S.C. § 102

The Examiner has rejected claims 1-10, 14, 18-21 and 24-26 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,703,957 to Morimoto et al., stating that Morimoto et al. disclose all of the limitations of these claims.

Without addressing the substance of the Morimoto et al. disclosure, Applicants note that the Morimoto et al. patent is not prior art relative to the present application. Applicants filed the present application on April 30, 2001. The "102(e) date" of the Morimoto et al. patent is its filing date of May 14, 2002, which is after April 30, 2001. Therefore, the Morimoto et al. patent is not a valid prior art reference under U.S.C. § 102(e). Nor is it a valid reference under any other section of 35 U.S.C. § 102. Consequently, Applicants respectfully request that the Examiner withdraw the present rejection.

References Made of Record, but Not Applied, by the Examiner

In the Office Action, the Examiner made of record, but did not apply, U.S. Patents Nos. 6,459,398 to Gureshnik et al., 6,317,067 to Mohindra and 6,081,150 to Yamaura et al. Applicants have reviewed these patents and assert that the present claims, as amended, are patentable over these references, alone and in combination with one another and/or other prior art references of record.

Independent claim 1, as amended, is directed to a DC voltage generator for generating a desired DC voltage level. The DC voltage generator includes a digital pulse modulation (DPM) generator generating a periodic bit-stream preconfigured to encode the desired DC voltage level

in the average value of the bit stream. The DC voltage generator also includes an analog averaging circuit that averages the bit-stream so as to generate a DC voltage that corresponds to the desired DC voltage level.

Relatedly, independent claim 19, as amended, is directed to a method of generating a desired DC voltage that includes selecting a desired DC voltage level, generating a period bit-stream that encodes the desired DC voltage level and averaging the periodic bit-stream so as to produce a DC voltage corresponding to the desired DC voltage level. As can be readily seen, each of amended independent claims 1 and 19 requires that the particular DC voltage produced correspond to a desired, i.e., predetermined, DC voltage level.

On the other hand, each of the Gureshnik et al., Mohindra and Yamaura et al. patents is directed to a digital to analog converter (DAC) that converts variable, i.e., non-desired or non-predetermined, digital signals into analog signals so that the information contained in the digital signal can be processed using analog components. While the configurations of the DACs of these patents are different from one another, none of the patents disclose or even suggest producing a desired DC voltage level from a bit-stream preconfigured to provide the desired DC voltage level. Consequently, none of the Gureshnik et al., Mohindra and Yamaura et al. DACs anticipate amended independent claims 1 and 19, nor claims 2-18 and 20-29 that depend therefrom.

In addition to amended independent claims 1 and 19 being patentable over the Gureshnik et al., Mohindra and Yamaura et al. patents and other prior art references of record, many of dependent claims 2-18 and 20-29 of the present application include limitations not disclosed or suggested by the references of record. Features of dependent claims 2-18 and 20-29 not disclosed or suggested by the references of record include: 1) a memory containing a series of bits that are cycled so as to generate the periodic bit stream; 2) a programming means for selecting the series of bits; 3) a PDM or PWM modulator that encodes the desired DC voltage level; 4) a circular shift register containing a series of bits that encodes the desired DC voltage level; and 5) a software based $\Sigma\Delta$ modulator programming means, among others.

Patentability of New Claims 30 and 31

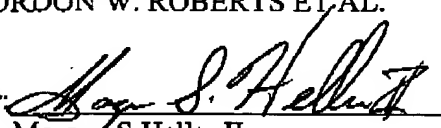
Each of new claims 30 and 31 requires, among other things, 1) a memory operatively configured to contain a series of bits encoding a desired DC voltage level and 2) a cycling circuit operatively configured to cycle the series of bits so as to generate an average DC voltage corresponding to the desired DC voltage level. None of the references of record, including the Gureshnik et al., Mohindra and Yamaura et al. patents, disclose or suggest these limitations. Again, e.g., each of the DACs disclosed by Gureshnik et al., Mohindra and Yamaura et al. operates on variable, i.e., non-desired or non-predetermined, digital signals and, thus, do not so much as suggest the memory-based cycling structure for generating a periodic bit-stream of new claims 30 and 31.

Conclusion

In view of the foregoing, Applicants respectfully submit that claims 1-31 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

GORDON W. ROBERTS ET AL.

By: 

Morgan S. Heller II
Registration No.: 44,756
Down Rachlin Martin PLLC
Tel: (802) 863-2375

Attorneys for Applicants

BTV.428943.1